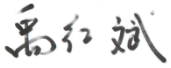
G83/2 Appendix 4 Type Verification Test Report

Type Approval and manufacturer/supplier declaration of compliance with the requirements of Engineering Recommendation G83/2.			
SSEG Type reference number	MI-500		
SSEG Type	Photovoltaic Microinverter		
System Supplier name	Hoymiles Converter Technology Co.,Ltd		
Address	3rd Floor,Building 11,18#Kangjing road,KangQiao Industrial Zone,HangZhou City,Zhejiang Province		
Tel	+86 571 28056101	Fax	+86 571 28056137
E:mail	bigyu@hzconverter.com	Web site	www.hoymiles.com
Maximum rated capacity, use separate sheet if more than one connection option.	Connection Option		
	0.5	kW single phase, single, split or three phase system	
	NA	kW three phase	
	NA	kW two phases in three phase system	
	NA	kW two phases split phase system	
SSEG manufacturer/supplier declaration			
I certify on behalf of the company named above as a manufacturer/supplier of Small Scale Embedded Generators, that all products manufactured/supplied by the company with the above SSEG Type reference number will be manufactured and tested to ensure that they perform as stated in this Type Verification Test Report, prior to shipment to site and that no site modifications are required to ensure that the product meets all the requirements of G83/2.			
Signed		On behalf of	Hoymiles Converter Technology Co.,Ltd
Note that testing can be done by the manufacturer of an individual component, by an external test house, or by the supplier of the complete system, or any combination of them as appropriate. Where parts of the testing are carried out by persons or organisations other than the supplier then the supplier shall keep copies of all test records and results supplied to them to verify that the testing has been carried out by people with sufficient technical competency to carry out the tests.			

Power Quality. Harmonics. The requirement is specified in section 5.4.1, test procedure in Annex A or B 1.4.1

SSEG rating per phase (rpp)			500	W	NV=MV*3.68/rpp	
Harmonic	At 45-55% of rated output		100% of rated output			
	Measured Value(MV) in Amps	Normalised Value (NV) In Amps	Measured Value(MV) In Amps	Normalised Value (NV) In Amps	Limit in BS EN 61000-3-2 in Amps	Higher limit for odd harmonics 21 and above
2	0.067	0.491	0.116	0.854	1.080	
3	0.020	0.146	0.030	0.222	2.300	
4	0.012	0.088	0.010	0.070	0.430	
5	0.008	0.060	0.005	0.039	1.140	
6	0.008	0.055	0.005	0.039	0.300	
7	0.006	0.046	0.004	0.026	0.770	
8	0.005	0.035	0.003	0.021	0.230	
9	0.005	0.035	0.002	0.013	0.400	
10	0.004	0.026	0.003	0.021	0.184	
11	0.004	0.026	0.002	0.018	0.450	
12	0.003	0.024	0.002	0.015	0.153	
13	0.003	0.023	0.002	0.018	0.210	
14	0.002	0.017	0.002	0.013	0.131	
15	0.003	0.018	0.003	0.024	0.150	
16	0.003	0.022	0.001	0.008	0.115	
17	0.002	0.016	0.002	0.013	0.132	
18	0.003	0.020	0.002	0.015	0.102	
19	0.002	0.015	0.003	0.018	0.118	
20	0.002	0.013	0.002	0.013	0.092	
21	0.003	0.021	0.000	0.001	0.107	

22	0.003	0.019	0.002	0.018	0.084	
23	0.002	0.017	0.001	0.007	0.098	0.147
24	0.002	0.014	0.001	0.007	0.077	
25	0.002	0.017	0.001	0.008	0.090	0.135
26	0.001	0.004	0.000	0.001	0.071	
27	0.001	0.008	0.002	0.018	0.083	0.124
28	0.001	0.004	0.003	0.018	0.066	
29	0.001	0.009	0.002	0.014	0.078	0.117
30	0.001	0.010	0.002	0.015	0.061	
31	0.001	0.007	0.002	0.012	0.073	0.109
32	0.002	0.015	0.000	0.001	0.058	
33	0.000	0.001	0.003	0.021	0.068	0.102
34	0.000	0.002	0.001	0.007	0.054	
35	0.002	0.012	0.002	0.014	0.064	0.096
36	0.002	0.012	0.002	0.015	0.051	
37	0.001	0.005	0.001	0.005	0.061	0.091
38	0.002	0.013	0.001	0.010	0.048	
39	0.001	0.010	0.001	0.005	0.058	0.087
40	0.001	0.009	0.003	0.018	0.046	

Note the higher limits for odd harmonics 21 and above are only allowable under certain conditions, if these higher limits are utilised please state the exemption used as detailed in part 6.2.3.4 of BS EN 61000-3-2 in the box below.

Power Quality. Voltage fluctuations and Flicker. The requirement is specified in section 5.4.2, test procedure in Annex A or B 1.4.3								
	Starting			Stopping			Running	
	dmax [%]	dc [%]	d(t) [%]	dmax [%]	dc [%]	d(t) [%]	Pst	Plt 2 hours
Measured Values	0.36	0.3	0	0.36	0.3	0	0.133	0.058
Normalised to standard impedance and 3.68kW for multiple units	2.65	2.21	0	2.65	2.21	0	0.98	0.43
Limits set under BS EN 61000-3-2	4%	3.30%	3.3% 500ms	4%	3.30%	3.3% 500ms	1	0.65
Test start date	2017-06-14			Test end date		2017-06-14		
Test location	No.8 Chunxin East Road, Wuxi, Jiangsu							

Power quality. DC injection. The requirement is specified in section 5.5, test procedure in Annex A or B 1.4.4				
Test power level	10%	55%	100%	
Recorded value(mA)	1.1229	2.6406	2.3144	
as % of rated AC	0.049%	0.115%	0.101%	
Limit	0.25%	0.25%	0.25%	

Power Quality. Power factor. The requirement is specified in section 5.6, test procedure in Annex A or B 1.4.2				
	216.2V	230V	253V	Measured at three voltage levels and at full output. Voltage to be maintained within ±1.5% of the stated level during the test.
Measured value	0.9955	0.9950	0.9940	
Limit	>0.95	>0.95	>0.95	

Protection. Frequency tests The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.3						
Function	Setting		Trip test		“No trip tests”	
	Frequency	Time delay	Frequency	Time delay	Frequency /time	Confirm no trip
U/F stage 1	47.5Hz	20s	47.5Hz	20.19	47.7Hz/ 25s	No trip
U/F stage 2	47Hz	0.5s	47.0Hz	0.541	47.2Hz/ 19.98s	No trip
					46.8Hz/ 0.48s	No trip
O/F stage 1	51.5Hz	90s	51.5Hz	90.0	51.3Hz/95s	No trip
O/F stage 2	52Hz	0.5s	52.0Hz	0.541	51.8Hz/ 89.98s	No trip
					52.2Hz/ 0.48s	No trip

Protection. Voltage tests The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.2						
Function	Setting		Trip test		“No trip tests”	
	Voltage	Time delay	Voltage	Time delay	Voltage /time	Confirm no trip
U/V stage 1	200.1V	2.5s	198.1V	2.531	204.1V/3.5s	No trip
U/V stage 2	184V	0.5s	182V	0.518	188V/2.48s	No trip
					180V/0.48s	No trip
O/V stage 1	262.2V	1.0s	264.2V	1.022	258.2V/2.0s	No trip
O/V stage 2	273.7V	0.5s	275.7V	0.515	269.7V/0.98s	No trip
					277.7V/0.48s	No trip
Note for Voltage tests the Voltage required to trip is the setting ±3.45V. The time delay can be measured at a larger deviation than the minimum required to operate the protection. The No trip tests need to be carried out at the setting ±4V and for the relevant times as shown in the table above to ensure that the protection will not trip in error.						

Protection. Loss of Mains test. The requirement is specified in section 5.3.2, test procedure in Annex A or B 1.3.4						
Note: Inverter tested according to BS EN 62116.						
Test Power and imbalance	33% -5% Q	66% -5% Q	100% -5% P	33% +5% Q	66% +5% Q	100% +5% P
Trip time. Limit is 0.5s	19.07ms	427.1ms	435.1ms	21.47ms	413.5ms	429.5ms

Protection. Frequency change, Stability test The requirement is specified in section 5.3.3, test procedure in Annex A or B 1.3.6				
	Start Frequency	Change	End Frequency	Confirm no trip
Positive Vector Shift	49.5Hz	+9 degrees		No trip
Negative Vector Shift	50.5Hz	- 9 degrees		No trip
Positive Frequency drift	49.5Hz	+0.19Hz/sec	51.5Hz	No trip
Negative Frequency drift	50.5Hz	-0.19Hz/sec	47.5Hz	No trip

Protection. Re-connection timer. The requirement is specified in section 5.3.4, test procedure in Annex A or B 1.3.5					
Test should prove that the reconnection sequence starts after a minimum delay of 20 seconds for restoration of voltage and frequency to within the stage 1 settings of table 1.					
Time delay setting	Measured delay	No reconnection when voltage or frequency is brought to just outside stage 1 limits of table 1.			
40s	40.3s	At 266.2V	At 196.1V	At 47.4Hz	At 51.6Hz
Confirmation that the SSEG does not re-connect.		No reconnection	No reconnection	No reconnection	No reconnection

Fault level contribution. The requirement is specified in section 5.7, test procedure in Annex A or B 1.4.6					
For a directly coupled SSEG			For a Inverter SSEG		
Parameter	Symbol	Value	Time after fault	Volts	Amps
Peak Short Circuit current	ip	N/A	20ms	14.60V	0.124A
Initial Value of aperiodic	A	N/A	100ms	5.85V	0.116A
Initial symmetrical	Ik	N/A	250ms	5.80V	0.114A
Decaying (aperiodic)	iDC	N/A	500ms	5.11V	0.109A
Reactance/Resistance Ratio	X/R	N/A	Time to trip	0.0012	(in seconds)

Self-Monitoring solid state switching The requirement is specified in section 5.3.1, No specified test requirements.	Yes/or NA
It has been verified that in the event of the solid state switching device failing to disconnect the SSEG, the voltage on the output side of the switching device is reduced to a value below 50 volts within 0.5 seconds.	N/A

Additional comments